What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of forming a copper damascene structure, said method comprising the steps of:

directly patterning a low-dielectric constant layer to form at least one opening through said low-dielectric constant layer;

forming a tungsten nitride layer by atomic-layer deposition using sequential surface reactions, said tungsten nitride layer being in contact with said at least one opening; and

providing a copper layer in said at least one opening.

2. The method of claim 1, wherein said low-dielectric constant layer includes a material selected from the group consisting of methylsilsequiazane, polyimide, spin-on-polymers, flare, polyarylethers, parylene, polytetrafluoroethylene, benzocyclobutene, SILK, fluorinated silicon oxide, hydrogen silsesquioxane and NANOGLASS.

3. The method of claim 1, wherein said low-dielectric constant layer comprises methylsilsequiazane.

4. The method of claim 3, wherein said step of forming said at least one opening further comprises patterning said low-dielectric constant layer.

5. The method of claim 4, wherein said step of patterning said low-dielectric constant layer further comprises exposing said low-dielectric constant layer to an electron beam or ultra violet light.

6. The method of claim 5, wherein said step of forming said at least one opening further comprises etching said low-dielectric constant layer with a tetra-methyl-ammonium hydroxide solution.

7. The method of claim 3, wherein said low-dielectric constant layer is formed by spin coating to a thickness of about 2,000 to 50,000 Angstroms.

8. The method of claim 7, wherein said low-dielectric constant layer is formed by spin coating to a thickness of about 5,000 to 20,000 Angstroms.

9. The method of claim 1, wherein said tungsten nitride layer is formed at a temperature of about 550-800K.

10. The method of claim 1, wherein said copper layer is selectively deposited by chemical vapor deposition.

11. The method of claim 10, wherein said copper layer is selectively deposited at a temperature of about 300°C to about 400°C.

12. The method of claim 11, wherein said copper layer is selectively deposited in an atmosphere of pure hydrogen from the β-diketonate precursor bis(6,6,7,8,8,8-heptafluoro-2,2-dimetyl 1-3,5-octanedino) copper (II).

13. The method of claim 11, wherein said copper layer is selectively deposited in an atmosphere of pure argon from the β-diketonate precursor bis(6,6,7,8,8,8-heptafluoro-2,2-dimetyl 1-3,5-octanedino) copper (II).

14. The method of claim 1, wherein said copper layer is formed by electroless deposition.

15. The method of claim 1 further comprising the act of chemical mechanical polishing said tungsten nitride layer.

16. The method of claim 1 further comprising the act of chemical mechanical polishing said copper layer.

17. A method of forming a copper damascene structure, said method comprising the steps of:

forming a material layer of methylsilsequiazane over a substrate;

forming at least one opening through said methylsilsequiazane layer;

forming a tungsten nitride layer by atomic-layer deposition using sequential surface reactions, said tungsten nitride layer being in contact with said at least one opening; and

providing a copper layer in said at least one opening.

18. The method of claim 17, wherein said step of forming said at least one opening further comprises directly patterning said methylsilsequiazane layer with a mask to form said at least one opening.

19. The method of claim 18, wherein said step of directly patterning said methylsilsequiazane layer further comprises exposing said methylsilsequiazane layer to an electron beam or ultra violet light.

20. The method of claim 19, wherein said step of forming said at least one opening further comprises etching said methylsilsequiazane layer with a tetra-methyl-ammonium hydroxide solution.

21. The method of claim 17, wherein said methylsilsequiazane layer is formed by spin coating to a thickness of about 2,000 to 50,000 Angstroms.

22. The method of claim 21, wherein said methylsilsequiazane layer is formed by spin coating to a thickness of about 5,000 to 20,000 Angstroms.

23. The method of claim 17, wherein said tungsten nitride layer is formed at a temperature of about 550-800K.

24. The method of claim 17, wherein said copper layer is selectively deposited by chemical vapor deposition.

25. The method of claim 24, wherein said copper layer is selectively deposited at a temperature of about 300°C to about 400°C.

26. The method of claim 25, wherein said copper layer is selectively deposited in an atmosphere of pure hydrogen from the β-diketonate precursor bis(6,6,7,8,8,8-heptafluoro-2,2-dimetyl 1-3,5-octanedino) copper (II).

27. The method of claim 25, wherein said copper layer is selectively deposited in an atmosphere of pure argon from the β-diketonate precursor bis(6,6,7,8,8,8-heptafluoro-2,2-dimetyl 1-3,5-octanedino) copper (II).

28. The method of claim 17, wherein said copper layer is formed by electroless deposition.

29. The method of claim 17 further comprising the act of chemical mechanical polishing said tungsten nitride layer.

30. The method of claim 17 further comprising the act of chemical mechanical polishing said copper layer.

31. A dual damascene structure comprising:

a substrate;

a metal layer provided within said substrate;

a methylsilsequiazane layer located over said substrate;

a via situated within said methylsilsequiazane layer and extending to at least a portion of said metal layer, said via being lined with a tungsten nitride layer and filled with a copper material; and

a trench situated within said methylsilsequiazane layer and extending to said via, said trench being lined with said tungsten nitride layer and filled with said copper material.

32. The dual damascene structure of claim 31, wherein said methylsilsequiazane layer has a thickness of about 2,000 to 50,000 Angstroms.

33. The dual damascene structure of claim 31, wherein said tungsten nitride layer has a thickness of about 50 to 200 Angstroms.

34. The dual damascene structure of claim 31, wherein said tungsten nitride layer is a sequential atomic layer deposition tungsten nitride layer.

35. The dual damascene structure of claim 31, wherein said substrate is a semiconductor substrate.

36. The dual damascene structure of claim 31, wherein said substrate is a silicon substrate.

37. A damascene structure comprising:

a substrate;

a metal layer provided within said substrate;

a methylsilsequiazane layer located over said substrate; and

at least one opening situated within said methylsilsequiazane layer and extending to at least a portion of said metal layer, said opening being lined with a tungsten nitride layer and filled with a copper material.

38. The damascene structure of claim 37, wherein said methylsilsequiazane layer has a thickness of about 2,000 to 50,000 Angstroms.

39. The damascene structure of claim 37, wherein said tungsten nitride layer has a thickness of about 50 Angstroms to about 200 Angstroms.

40. The damascene structure of claim 37, wherein said tungsten nitride layer is a sequential atomic layer deposition tungsten nitride layer.

41. The damascene structure of claim 37, wherein said copper material includes copper or a copper alloy.

42. The damascene structure of claim 37, wherein said substrate is a semiconductor substrate.

43. The damascene structure of claim 37, wherein said substrate is a silicon substrate.

44. A processor-based system comprising:

a processor; and

an integrated circuit coupled to said processor, at least one of said processor and integrated circuit including a damascene structure, said damascene structure comprising a metal layer over a substrate, a methylsilsequiazane layer over said metal layer, and at least one opening situated within said methylsilsequiazane layer and extending to at least a portion of said metal layer, said opening being lined with a tungsten nitride layer and filled with copper.

45. The processor-based system of claim 44, wherein said processor and said integrated circuit are integrated on same chip.